REMARKS

The present application was filed on December 18, 2001 with claims 1 through 22. Claims 1 through 22 are presently pending in the above-identified patent application. Claims 3-6, 11, 13 and 14 have been proposed to be cancelled herein, without prejudice. Claims 1, 8, 12, 16 and 21 are proposed to be amended herein. Claims 23-29 are proposed to be added herein.

In the Office Action, the Examiner objected to claim 5 as being of improper dependent form for failing to limit the subject matter of a previous claim. The Examiner rejected claims 16-19 and 22 under 35 U.S.C. §102(e) as being anticipated by Raghavan (United States Patent No. 6,418,172). In addition, the Examiner rejected claims 1-9, 11-15, 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Heegard (United States Patent Number 6,961,392). The Examiner rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Raghavan and Heegard and further in view of Liao (United States Patent Number 5,546,430).

Claim 5

The Examiner objected to claim 5 as being of improper dependent form for failing to limit the subject matter of a previous claim. Claim 5 has been cancelled herein, without prejudice.

Claim 16-19

Claims 16-19 and 22 were rejected under 35 U.S.C. §102(e) as being anticipated by Raghavan. The Examiner asserts that Raghavan discloses a method for representing an MLT-3 code as a trellis, said MLT-3 code using three signal levels to represent two binary values, the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a previous symbol period; and generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values. (citing FIG. 1A and col. 3, lines 37-50).

Raghavan, however, discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG. 1A).

Independent claim 16 has been amended to emphasize that a first binary value, such as logic 1, causes a transition of the MLT-3 signal, and a second binary value, such as logic 0, leaves the MLT-3 signals unchanged. Support for this amendment can be found in the original specification, for example, at page 4, lines 17-18. Contrast, for example, the labels for the transitions in the trellis shown in FIG. 4 of the present application and FIG. 1A of Raghavan.

Thus, Raghaven does not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value causes a state transition in said trellis and a second binary value does not cause a state transition in said trellis," as required by claim 16, as amended.

Independent Claims 1 and 8

Independent claims 1 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Heegard. Regarding claims 1 and 8, the Examiner asserts that Raghavan discloses generating at least one trellis representing an MLT-3 code and a dispersive channel. The Examiner acknowledges that Raghavan does not disclose performing joint equalization and decoding of the received signal using the trellis but cites Heegard for this purpose (citing the Abstract, FIGS. 4 and 5; col. 8, line 1, to col. 9, line 28).

Raghavan, however, does not disclose or suggest generating at least one trellis representing both an MLT-3 code and a dispersive channel, as required by independent claim 1 and 8, as amended. See, for example, FIG. 1A of Raghavan showing just a MLT-3 encoder trellis. Applicants can find no disclosure or suggestion in Raghavan to generate a trellis representing *both* the MLT-3 code and dispersive channel.

Dependent Claims 2-7, 9-15 and 17-22

Dependent claims 17-19 and 22 were rejected under 35 U.S.C. §102(e) as being anticipated by Raghavan; dependent claims 2-7, 9, 11-15, 20 and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Heegard; and dependent claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan and Heegard and further in view of Liao. Claims 2-7, 9-15 and 17-22 are dependent on claims 1, 8, and 16, respectively, and are therefore patentably distinguished over Raghavan, Heegard and Liao (alone

or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

With regard to Claim 10, for example, the Examiner asserts that Heegard disclose that the reduced complexity sequence estimator further comprises a branch metric units (BMU) that calculates branch metrics based on the received signal (citing FIG. 5, block 520, col. 8, line 36, to col. 9, line 14); an add-compare-select unit (ACSU) that determines the best surviving paths into the reduced states (citing FIG. 5, block 500, col. 8, line 36, to col. 9, line 14); a survivor memory unit (SMU) that stores the best surviving paths (citing FIG. 5, block 510, col. 8, line 36, to col. 9, line 14); and a decision-feedback unit (DFU) that takes survivor symbols from the SMU to calculate ISI estimates for the reduced complexity (citing FIG. 5, block 510, col. 8, line 36, to col. 9, line 14), wherein the ISI estimates are used by the BMU to calculate branch metrics for transitions in the reduced-state trellis (citing FIG. 5, block 520, col. 8, line 36, to col. 9, line 14).

The Examiner acknowledges that Raghavan and Heegard do not disclose that the reduced complexity sequence estimation technique is a reduced number of states, but cites Liao for this purpose.

Among other differences, block 500 in Figure 5 of Heegard is not an ACSU. As explicitly set forth in Claim 10, the ACSU "determines the best surviving paths into the reduced states." It is well understood by those of ordinary skill in the art that an ACSU performs the well-known add-compare-select operation. Block 500 in Heegard, however, is a Fano state machine module that determines which branch the symbol estimator should proceed on and whether to proceed back or forward based on comparisons between path metrics and thresholds (see, e.g., col. 9, lines 7-14). An "ACSU," however, *adds* path metrics and branch metrics for path extensions into a state, *compares* these path metrics and *selects* the path with the minimum path metric as survivor path. Heegard does not disclose that block 500 performs these functions.

Likewise, the symbol estimator 510 in Heegard is not a SMU and does **not** "store the best surviving paths," as expressly required by claim 10. Rather, block 510 generates an estimate of a channel output by adding the multipath terms obtained from previous estimates of

modulation symbols and the FIR channel coefficients (see, e.g., column 8, lines 56-60). The functionality of the symbol estimator 510 is therefore different from the claimed SMU.

Furthermore, the symbol estimator 510 is not a DFU. Heegard does not disclose that the symbol estimator 510 takes survivor symbols from the SMU to compute ISI estimates for reduced states, as further required by claim 10. Survivor symbols are defined in the present specification as symbols from the survivor path into a trellis state. See, e.g., page 6, lines 16-21, and page 7, lines 7-12, as well as original claim 10. Heegard does not disclose computing ISI estimates using survivor symbols, but merely discloses generating an estimate of a channel output based on previous estimates of modulated symbols.

The Examiner makes similar assertions regarding claim 12. The Examiner is referred to the above argument regarding claim 10 which is applicable to claim 12 for the corresponding limitations.

With regard to claim 21, the Examiner asserts that Raghavan and Heegard disclose concatenating the trellis with a trellis representing a channel to obtain a super trellis (citing FIG. 1; col. 1, line 56, to col. 2, line 5; col. 6, line 41, to col. 7, line 7). Heegard, however, does not disclose combining the MLT-3 trellis with a trellis representing a channel to obtain a super trellis, as required by claim 21. FIGS. 1A and 1B and col. 6, line 41 to col. 7, line 7 merely describe the encoder and the finite state machine for a BCC encoder. Col. 1, line 56, to col. 2, line 5 merely describes search based decoding.

New Claims

New claims 23-29 are directed to various aspects of the invention. New claims 23-29 have been added to more particularly point out and distinctly claim various features of the invention, consistent with the scope of the originally filed specification, in order to give applicants the protection to which they are entitled. No new matter has been introduced. For example, new claims 23 and 27 recite that "a state in said trellis is given by a concatenation of said MLT-3 code state and said channel state, wherein said channel state describes said dispersive channel." Support for this feature is found, for example, at page 5, lines 4-8 of the originally filed specification.

New claims 24 and 28 recite that "a state in said trellis is given by a concatenation of said MLT-3 code state and a truncated channel state, wherein said truncated channel state partially describes said dispersive channel." Support for this feature is found, for example, at page 6, lines 9-21, of the originally filed specification.

New claim 25 recites the additional steps of "computing ISI estimates for said states using symbols from corresponding survivor paths; computing branch metrics for transitions in said trellis based on said ISI estimates; determining survivor paths into said states based on said branch metrics; and storing said survivor paths." Support for this feature is found, for example, at page 7, lines 7-18, of the originally filed specification.

New claims 26 and 29 recite that "a number of states in said trellis is given by $4x(2^K)$, where K is the truncated channel memory." Support for this feature is found, for example, at page 6, lines 9-21, of the originally filed specification.

Conclusion

All of the pending claims, i.e., claims 1-29, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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